Remarks

Claims 1-16 are pending in the application. Claims 1-4, 6-10 and 13-16 stand rejected. Claims 5, 11 and 12 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. By this response, claims 1, 4, 7 and 10 have been amended and claims 3, 5 and 11 have been canceled. Applicants respectfully request reconsideration of all pending claims herein.

Claim Objections

The Examiner objected to claims 5, 11 and 12 as being dependent upon a rejected base claim, but indicated such claims would be allowable if rewritten to include all the limitations of the base claim and any intervening claims. Accordingly, Applicants have canceled claims 3 and 5 and amended claim 1 to include the limitations of claim 5 and intervening claim 3, therefore claim 1 as amended is allowable. Applicants have canceled claim 11 and amended claim 10 to include the limitations of claim 11, therefore claim 10 as amended is allowable as is claim 12, which depends from claim 10 as amended.

The Examiner objected to claim 1 stating that the first occurrence of a period should replaced with a comma. Applicants have amended claim 1 to replace the first occurrence of a period with a semicolon.

The Examiner objected to claim 3 indicating that it is unclear whether the recited DRAMs refer to the DRAMs recited in claim 1. Applicants have amended claim 3 to so indicate.

The Examiner objected to claim 7 indicating that it is unclear whether the "means for changing modes" is part of the memory controller or the memory system. Accordingly, Applicants have amended claim 7 by replacing the recitation of a "means for changing modes" with "a logic element integral to the memory controller that is responsive to the programmable pin."

Accordingly, Applicants respectfully submit that the Examiner's objection to claims 3, 5, 7 and 10-12 has been overcome.

Claim Rejections - 35 U.S.C. § 102(e)

The Examiner rejected claims 6-8 under 35 U.S.C. § 102(e) as being anticipated by U.S Patent No. 6,414,868 to Wong, et al. The Examiner stated that Wong discloses similar elements in Figures 2, 3 and 5 corresponding to the limitations of Applicants' claimed memory system directed to the ability to accept non-inverting and inverting input as well as a memory controller capable of driving either non-inverted or inverted signals to the DRAMs as configured with a programmable pin.

Applicants respectfully submit that Wong is directed to a memory expansion module incorporating control logic that facilitates switching from an upper bank of memory chips to a lower bank of memory chips. (Wong at Col. 2, lines 39-55; and Claim 1) Wong's bank control circuit 2000 facilitates communication with multiple memory banks without increasing the number of address inputs to the memory system. (Wong at Col. 1, lines 62-67 – Col. 2, line 1) In this regard, Wong's system enables memory expansion of a computer system using memory chips with the same capacity. (Wong at Col. 2, lines 34-38)

Conversely, Applicants' memory system "reduces the maximum count of drivers that will be switching in any one direction at a time, by utilizing a memory device that is designed to accept inverted inputs when so programmed." (Applicants' Specification at Paragraph 25) Applicants respectfully submit that Wong does not anticipate or suggest Applicants recited memory system because Wong is directed to a fundamentally different structure and function. Moreover, the use of inverting logic shown in Figure 5 of Wong represents the logic required to select a particular bank of memory rather than directing inverting inputs to the memory. As such, Applicants respectfully submit that the memory system claimed herein is not anticipated or suggested by Wong.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described in a single prior art reference. (MPEP §2131) Applicants respectfully submit that Wong does not teach or suggest Applicants' claimed memory system in which a memory controller responsive to a programmable pin directs selected banks of the memory to accept either a non-inverting or an inverting input to reduce simultaneous switching noise. (Applicants' Specification at Paragraph 22) Indeed, there is no teaching in Wong regarding modulating the logic polarity of selected memory bank inputs. Accordingly, Applicants respectfully submit that Wong does not anticipate the memory system claimed herein.

Claim 7 as amended and claim 8 depend from claim 6. For the reasons noted above independent claim 10 as amended is allowable. Claims 12-14 depend from claim 10 as amended. Therefore, Applicants respectfully submit that the Examiner's rejection of claims 6-8 and 10 and 12-14 under 35 U.S.C. § 102(e) has been overcome.

The Examiner rejected claims 15 and 16 under 35 U.S.C. § 102(e) as being anticipated by U.S Patent No. 6,414,868 to Wong, et al. The Examiner stated that Wong discloses a control circuit capable of conveying a plurality of inverted and non-inverted signals operable in the normal mode, such as accessing a memory data; and redrive circuitry which generates an output in both non-inverted and inverted polarity signals form one or more input signals. (1st OA at p. 6, citing Wong at Col. 1, lines 30-55) Applicants respectfully submit that the inverting and non-inverting control signals disclosed in Fig. 5 of Wong are exclusive to the bank selection logic of the bank control circuit 2000. That is, the inverting and non-inverting logic shown are not propagated to the memory address inputs but merely control which banks are selected. As such, Wong does not suggest or teach each element of claims 15 and 16. Accordingly, Applicants respectfully submit that the Examiner's rejection of claims 15 and 16 under 35 U.S.C. § 102(e) has been overcome.

Claim Rejections - 35 U.S.C. § 103(a)

The Examiner rejected claims 3 and 4 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,414,868 to Wong in view of U.S. Patent No. 6,693,483 to Deml. In respect to Wong, the Examiner stated that Wong discloses similar elements in Figures 2, 3 and 5 corresponding to the limitations of Applicants' claimed memory system directed to the ability to accept non-inverting and inverting input as well as a memory controller capable of driving either non-inverted or inverted signals to the DRAMs as configured with a programmable pin. The Examiner notes that Wong is silent on the issue of whether a DRAM may be operated in either a non-inverting or inverting mode (1st OA at p. 7) and indicates that Deml shows that it is well known and necessary to have high positive and also negative voltages [non-inverted and inverted modes] applied to DRAMs during operation. (1st OA at p. 7)

As noted above, the inverting and non-inverting logic shown in Fig. 5 of Wong merely controls which memory banks are selected and therefore does not anticipate Applicants' invention herein. Wong teaches a memory expansion module incorporating control logic that facilitates switching from an upper bank of memory chips to a lower bank of memory chips. (Wong at Col. 2, lines 39-55; and Claim 1) Wong's bank control circuit 2000 facilitates communication with multiple memory banks without increasing the number of address inputs to the memory system. (Wong at Col. 1, lines 62-67 – Col. 2, line 1)

Applicants respectfully submit that Deml, on the other hand, is directed to a charge pump design that has no bearing to the subject matter of Applicants' invention. Deml does not suggest or motivate the use of non-inverting and inverting logic on different memory banks of a memory system to reduce the latency caused by simultaneous switching. The statement cited by the Examiner (Deml at col. 1, lines 21-27) merely notes the necessity of high positive and negative voltages from time to time in memory operation but provides no indication of what or how those voltages are used. Applicants respectfully submit that Deml teaches a charge pump design capable of compensating for operating conditions by varying the number of stages. (Deml at col. 2, lines 45-59).

Applicants respectfully submit that no motivation exists to combine Wong with Deml. The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. (MPEP §2143.01) As such, a prima facie case of obviousness has not been established. Therefore, Applicants respectfully submit that the Examiner's rejection under 35 U.S.C. § 103(a) has been overcome.

Allowable Subject Matter

Applicants gratefully acknowledge the Examiner's indication of allowable subject matter with respect to claims 5, 11 and 12, stating that such claims would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Accordingly, Applicants have canceled claims 3 and 5 and amended claim 1 to include the limitations of claim 5 and intervening claim 3, therefore claim 1 as amended is allowable. Claims 2 and 9 depend from claim 1 as amended. Therefore, claims 1, 2, 4 and 9 are in condition for allowance.

Applicants have canceled claim 11 and amended claim 10 to include the limitations of claim 11, therefore claim 10 as amended is allowable. Claims 12-14 depend from claim 10 as amended. Therefore, claims 10-14 are in condition for allowance.

Applicants respectfully submit that the Examiner's objections have been overcome and claims 1, 2, 4, 9 and 10-14 are in condition for allowance.

Prior Art Made of Record

The prior art made of record by the Examiner and not relied upon, i.e. Hamamatsu, et al. (U.S. Patent App. No. 2003/0035328); and Tamura, et al. (U.S. Patent No. 6,493,394) have been reviewed and Applicants respectfully submit that the references cited do not anticipate or suggest the elements of pending independent claims 1, 6, 10, 15 and 16.

Conclusion

Based on the foregoing, it is respectfully submitted the application may be passed to issuance.

The Examiner is urged to call the undersigned at the number listed below if, in the Examiner's opinion, such a phone conference would aid in furthering the prosecution of this application.

Respectfully submitted,
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